Open Source Embedded Vision Sensors

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Centeye, Inc.

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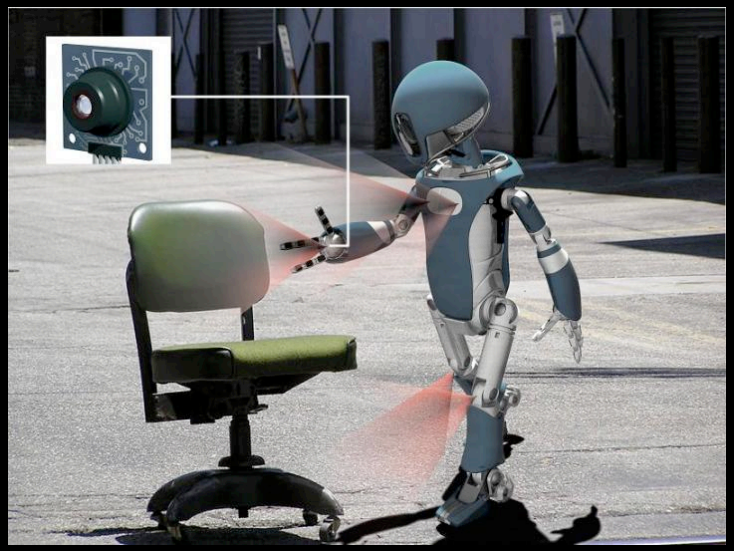
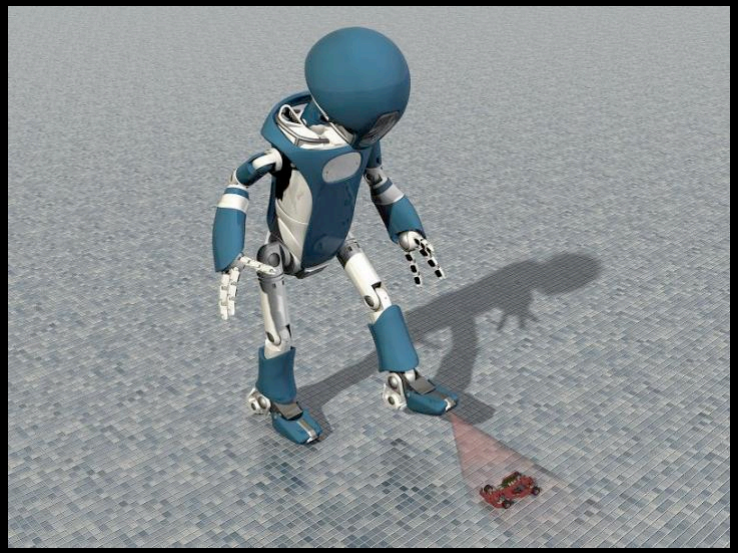
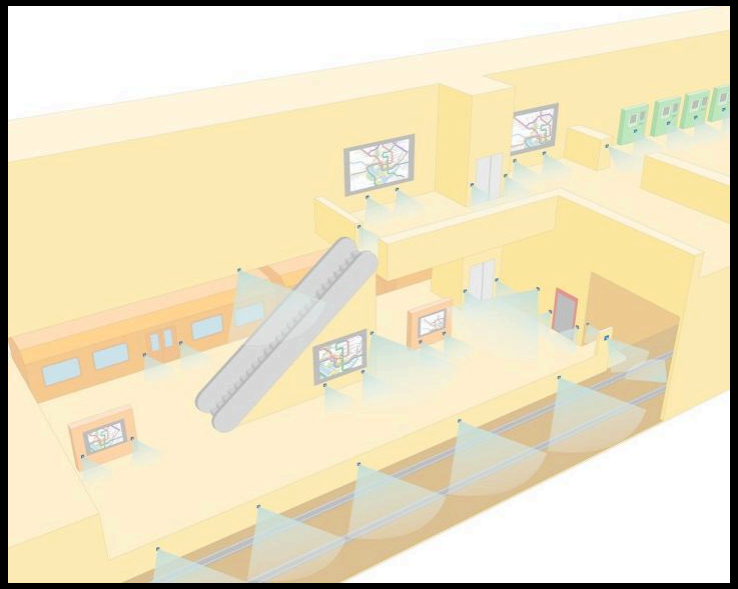
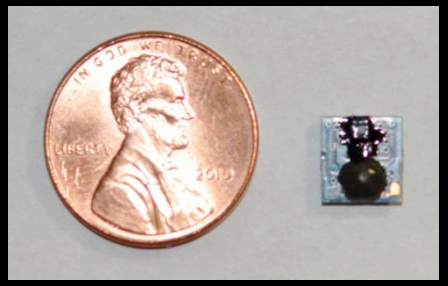
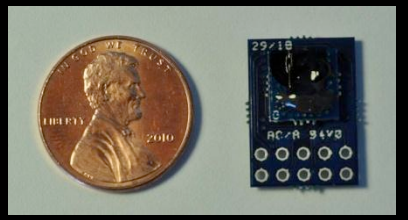
Embedded Vision Sensors

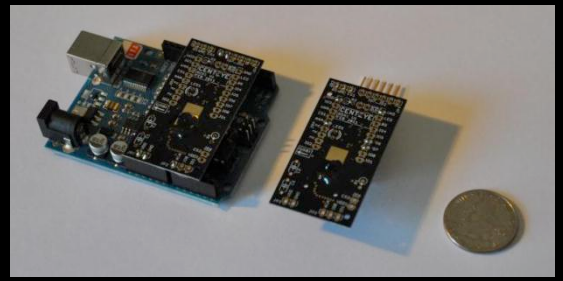












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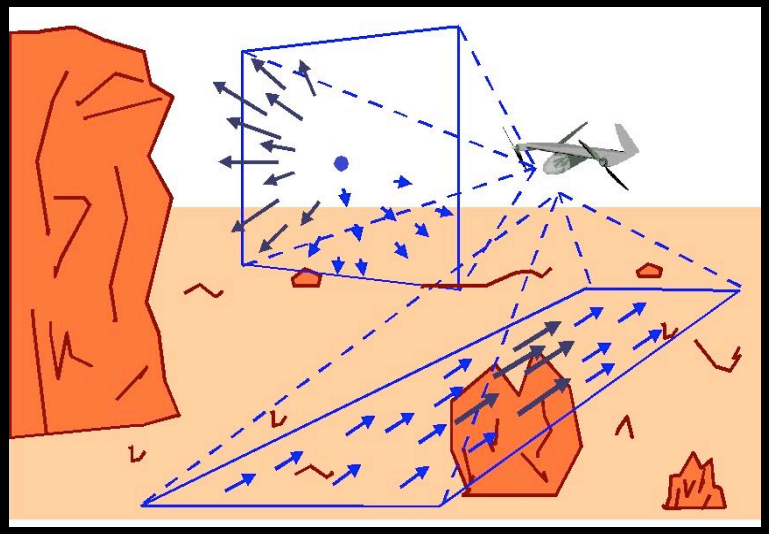
Part 1: Why are opening up our hardware

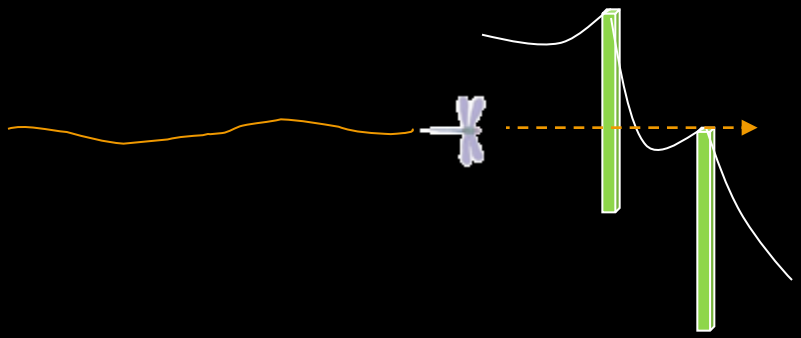
Part 2: Reconciling chip design and open source

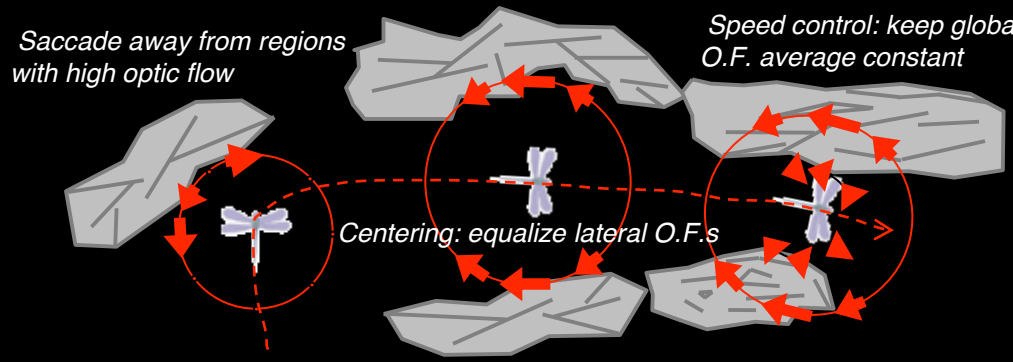
My Obsession (since 1996)



Major Goal:

Use optical flow and other vision techniques to allow a small robotic aircraft to fly through an environment without crashing into obstacles





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2001

http://www.youtube.com/watch?v=EkFh_2UX-Jw

16 pixels, PIC18C252, 2MIPS

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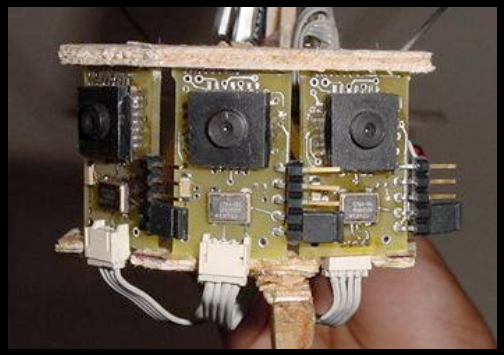
2003

http://www.youtube.com/watch?v=Ah-eESVigd4



3 X (88 pixels, PIC18F, 10MIPS)

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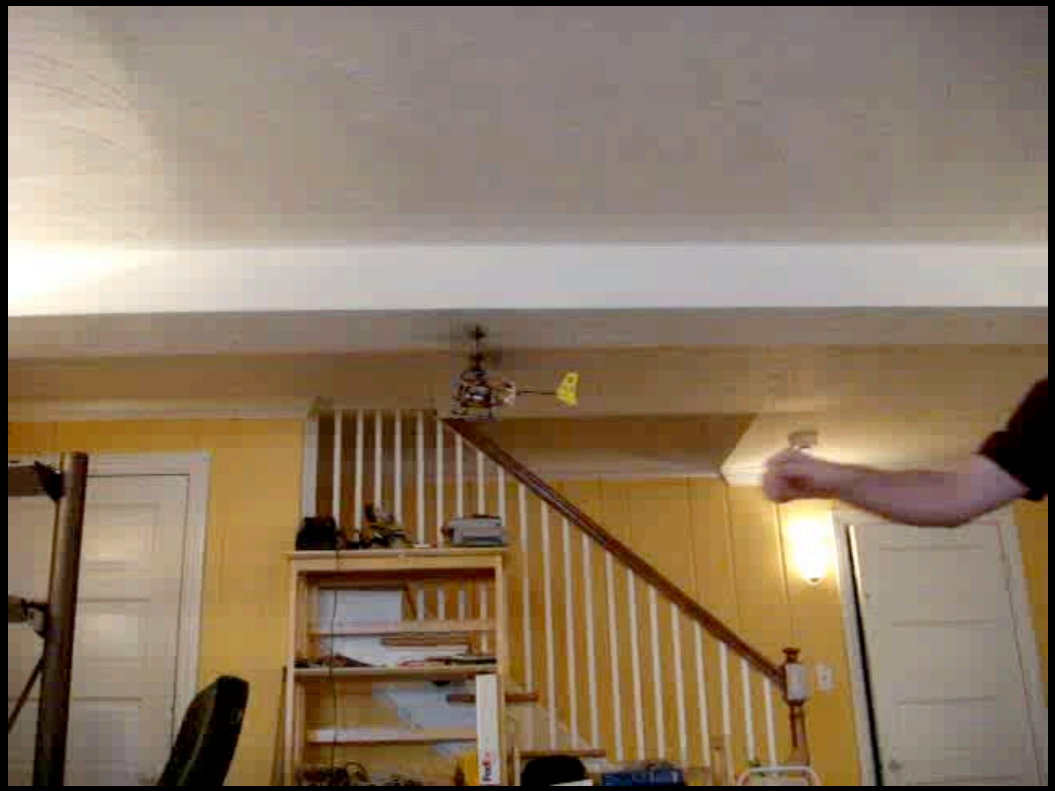
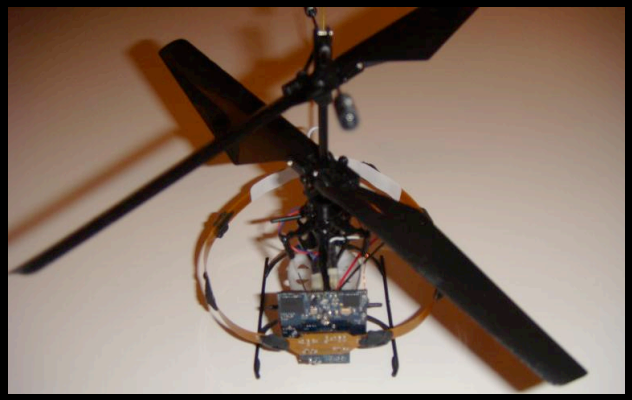
2009





http://www.youtube.com/watch?v=pwjUcFQ9b3A

512 pixels, Atmel AVR32, 60MHz, 3.0g

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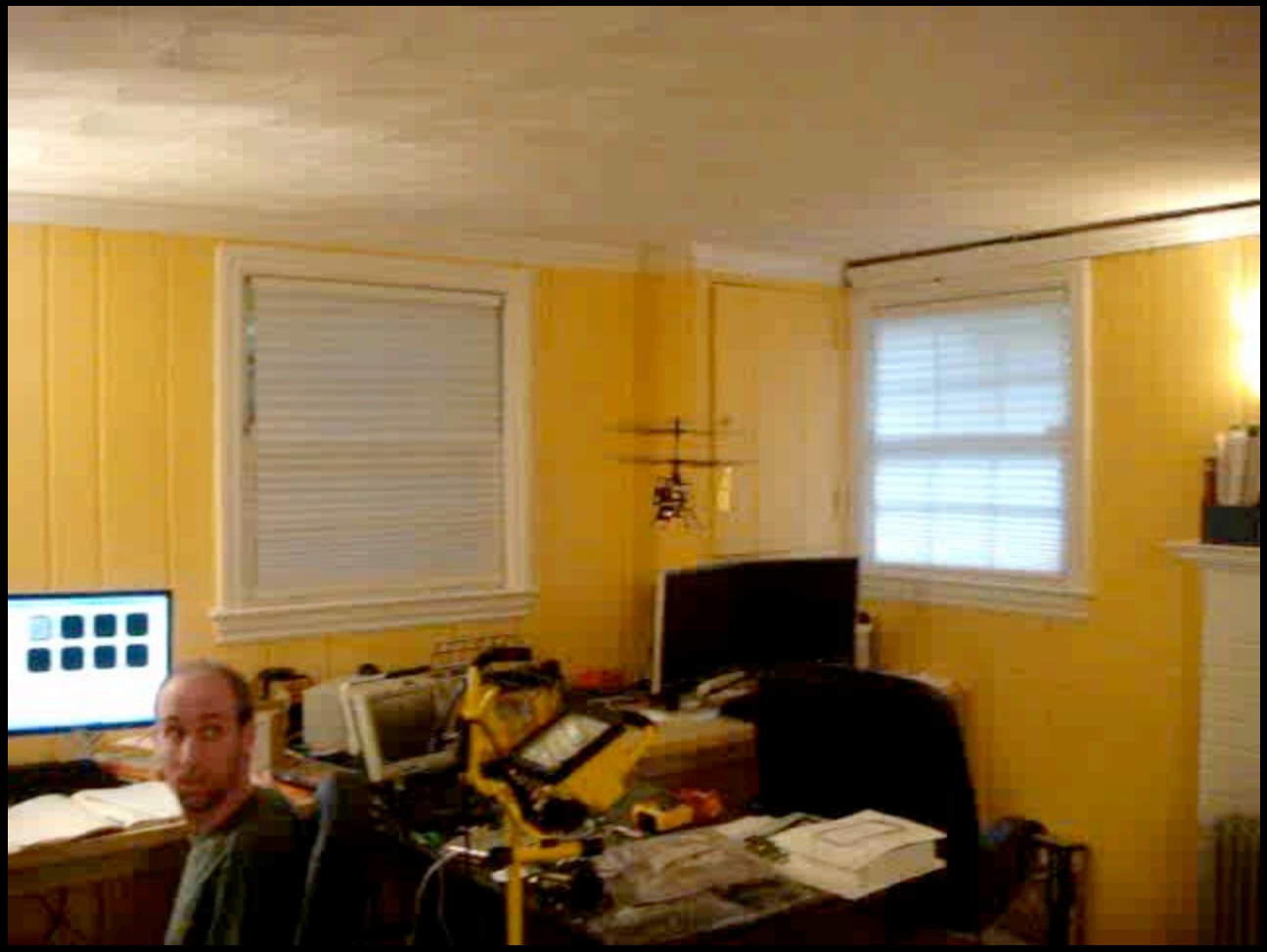
2009



http://www.youtube.com/watch?v=AoKQmF13Cb8

8 pixels!

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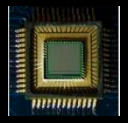
“If we knew what we were doing, it wouldn’t be research!”

-Albert Einstein

http://www.youtube.com/watch?v=dDbazL5Ipll

Vertically Integrated Approach

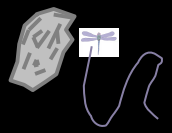
Optics



“Vision Chip”

Vision sensor

Image processing



Control algorithms

Vehicle

- Split processing between optics, circuitry, and algorithms as appropriate
- Optimize to figures of merit that really matter as opposed to arbitrary metrics
- Control the interface- optimize them instead of being constrained by some industrial standard
- Include useful features
- Eliminate unnecessary features
- Eliminate unnecessary pixels!!

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And so why open source?

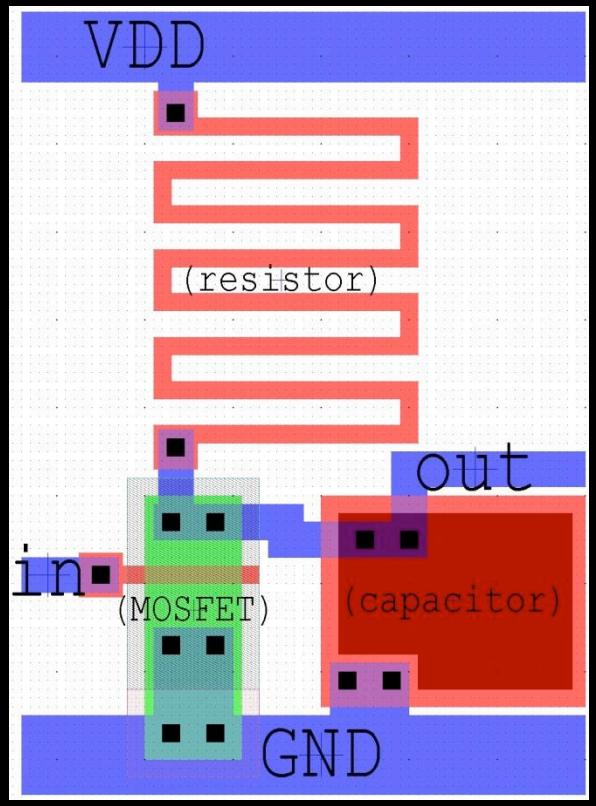
We have experience with the vertically integrated approach
… and others do not.

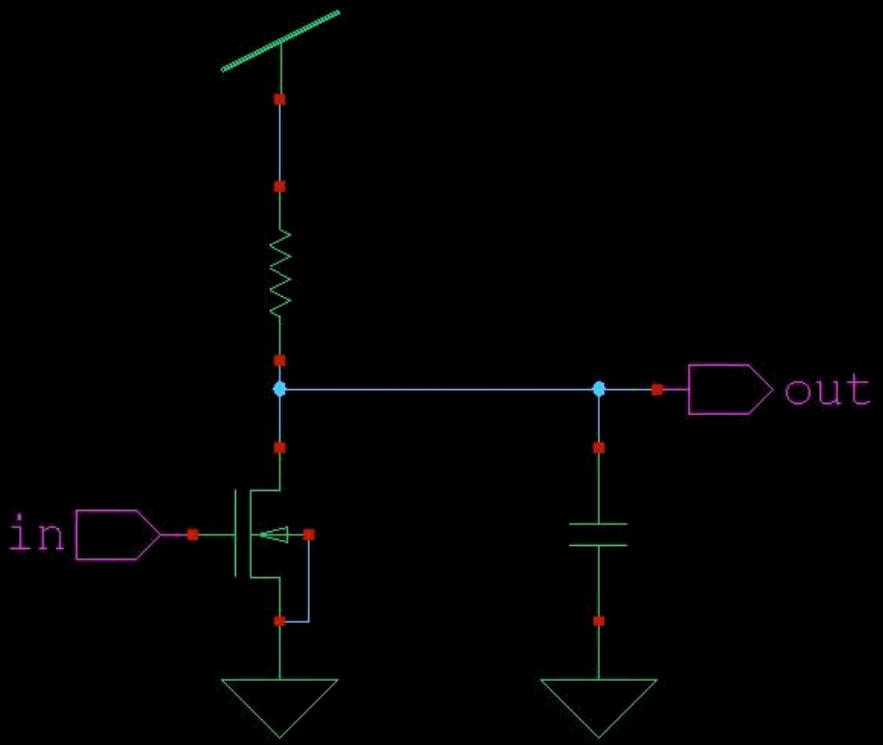
Therefore:
•It is very difficult to convey exactly what our technology “is”
•Things that are obvious to us are not to others
(We are not smarter than others- we just have experience…)

Why open source hardware?
•We need to make it easy for others to tinker and experiment
•Transparency and openness is the only way to encourage this
•Our technology is both software and hardware

Basic Chip Design

You draw both the connections and the components!

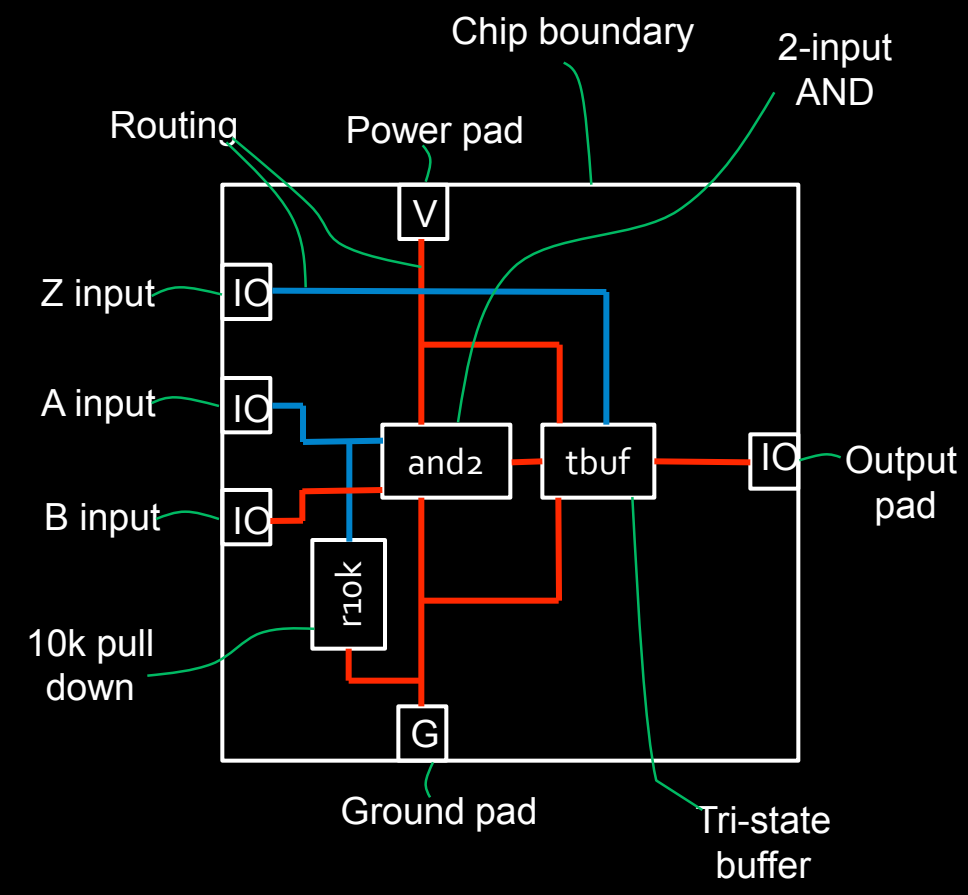




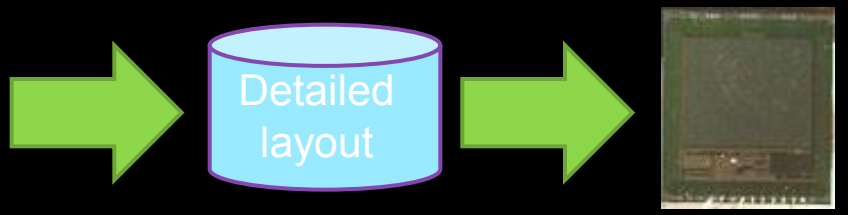
The problem: Design rule files and library files for chip design are generally NOT open!

Is “Partially Open” a Possibility?

Well, it is possible, but would the community accept it?



1. Designer creates abstract layout



2. “Middleman” or foundry generates native level layout

3. Fabricate!

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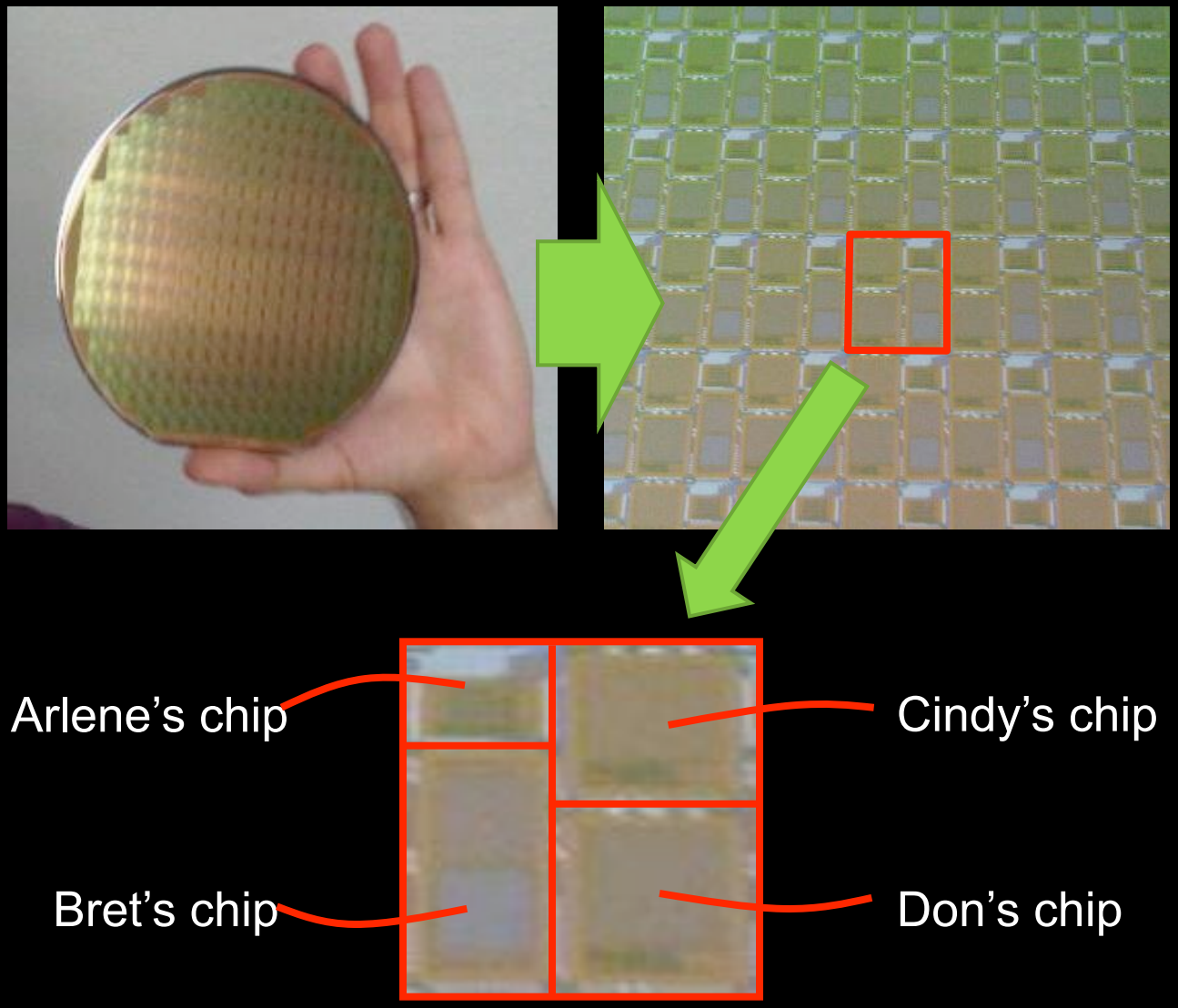
Batch Fabrication of Chips is Pretty Common



The Numbers: Hypothetical Batch Chip Fab

Cost for a fab on a 0.6um process: $35,000
- $20,000 for the mask set
- $10,000 for a batch of 10 x 6” wafers
  - Note: About 30+ reticles per wafer or 300+ reticles total
- $5,000 for dicing

Scenario: Get 100 customers to contribute 100 different designs
- Reticle = 21mm x 21mm → 2mm x 2mm for each design
- Total fab cost per customer for chips = $350 (for 300 chips!)
- Add $100 per customer for packaging (5 chips in DIP packages)
- Total cost per customer: About $450
- If we multiply by 2.6, we bill the customer $1170

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Thank You!!!

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